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<u>L21</u>	L18 and target\$4	28	<u>L21</u>
<u>L20</u>	L18 and l11	7	<u>L20</u>
<u>L19</u>	L18 and l10	22	<u>L19</u>
<u>L18</u>	l15 and (micro\$) near3 (control\$5 or sequenc\$4 or engine\$1)	34	<u>L18</u>
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<u>L15</u>	L14 and hardware near8 (thread\$3 or multi\$7 near4 thread\$3)	131	<u>L15</u>
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<u>L12</u>	L11 and l5	9	<u>L12</u>

<u>L11</u>	(712/231-248)[CCLS]	2869	<u>L11</u>
<u>L10</u>	(712/2-300)[CCLS]	11247	<u>L10</u>
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<u>L8</u>	l1 and branch\$6 near8 address\$3	58	<u>L8</u>
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<u>L5</u>	l1 and branch\$6	241	<u>L5</u>
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IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

**1. Design and fabrication of silicon micro components**

Buttgenbach, S.;

Micromechatronics and Human Science, 2002. MHS 2002. Proceedings of 2002 International Sym;
20-23 Oct. 2002 Page(s):9 - 16

Digital Object Identifier 10.1109/MHS.2002.1058003

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Citation



Citation & Abstract

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

**1. ETA: experience with an Intel Xeon processor as a packet processing engine**

Regnier, G.; Minturn, D.; McAlpine, G.; Saletore, V.A.; Foong, A.;

Micro, IEEE

Volume 24, Issue 1, Jan.-Feb. 2004 Page(s):24 - 31

Digital Object Identifier 10.1109/MM.2004.1268989

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